A TECHNIQUE FOR THE MAINTENANCE OF FET POWER AMPLIFIER EFFICIENCY UNDER BACKOFF

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ABSTRACT

An operational technique for FET power amplifiers, which allows the maintenance of high efficiency as the amplifier is backed off from its rated output power level, is described. Using this technique, an experimental, single-stage, 1-W, C-band amplifier, capable of 65 percent power-added efficiency at its rated output power, maintains a minimum efficiency of 55 percent for a 10-dB output backoff range. Comparable amplifiers operating under conventional Class B or Class A demonstrate efficiencies of about 18 and 4 percent, respectively. An analytic basis for the technique is given. Experimental results are also presented for a three-stage, 2-W, C-band amplifier.

INTRODUCTION

A fundamental goal of phased-array antenna development both for communications and radar applications is the realization of low-cost, high-efficiency active modules. High-efficiency operation is critical because of limited prime power and, in many applications, the difficulties associated with heat removal. Transmitter amplifiers in phased arrays, moreover, are often not operated at their maximum efficiency either because of the requirements of achieving a prescribed amplitude taper, the need to operate under reduced power conditions and/or, in multimode applications, the need to vary the taper dynamically. The result is a significantly degraded system efficiency. The alternative of developing, manufacturing, and stocking different amplifiers for different locations in the array is costly and logistically undesirable. The ideal solution is a single power amplifier that can maintain high efficiency over a wide range of output powers and thus be usable in all locations in the array and at various drive levels. Conventional Class B operation is a partial solution. It improves overall efficiency and reduces the efficiency degradation with backoff compared with that experienced with Class A amplifiers. This degradation, even with Class B, is nevertheless substantial and has the effect of reducing the overall operating efficiency of phased-array systems.

DESCRIPTION OF TECHNIQUE

Techniques involving bias modification as a function of RF drive for the purpose of linearization [1] and efficiency improvement [2] have been previously reported. With at least one exception at audio frequencies [3], little has been published on the application of this technique for the purpose of efficiency improvement under backoff.

The technique developed and analyzed here consists of the modification of the drain and gate bias voltages as a function of output power backoff, together with a reduction in input RF drive. This concurrent modification of DC bias and RF drive allows maximum modulation of the allowed device drain voltage and current at any given drive level and thus maintains the device in a state of "extended saturation" (in which maximum efficiency is achieved) over a large output power range. The external load impedance is not varied. The technique is equally applicable to all classes of device operation, although Class B is the preferred approach in most cases, including the one described here. Figure 1 shows qualitatively a typical FET characteristic. The load line representing operation at maximum power, together with the device characteristic, determines the allowed excursions of drain current and voltage and, thus, output power. A reduction in RF drive under fixed-bias conditions does not allow the DC component of the drain current to drop proportionally to the RF components. This is obvious in the Class A case, but is also true, to a lesser degree, in the Class B case. If, however, the drain bias is reduced as the RF drive is reduced, as depicted by the load line to the left, the DC component can be reduced substantially, thus improving the efficiency while still allowing the voltage and current excursions for the required output power. In addition to the reduction in drain voltage, a

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small increase (more positive) in gate voltage is helpful in increasing the average g_m, thus increasing gain and power-added efficiency.

In a system implementation, the drain and gate voltages may be controlled by various means. Two possible configurations are illustrated in Figure 2. Figure 2a represents a simplified system in which a sample of the input power is detected, amplified, and used to select the appropriate bias states from a lookup table. Figure 2b is similar, except that the bias and VVA voltages are controlled by a computer-generated command. Both implementations require a priori knowledge of the bias/power relation and its availability as a lookup table. The efficiency of the bias controller will, of course, effect the overall efficiency of the system. The incremental increase in complexity required to implement this technique should, however, have minimal effect on overall efficiency.

Figure 3 shows the remarkable improvement in the measured power-added efficiency of a Class B amplifier operated in this mode, compared with the more conventional fixed-bias approach.

For the experimental Class-B single-stage amplifier used here and exhibiting a power-added efficiency of 65 percent at optimum drive (1 W out) [4], the efficiency is 57 percent at 10-dB backoff both with drain and gate bias modification, 49 percent with only drain voltage modification, and 18 percent with conventional fixed biasing. A Class A amplifier would exhibit an efficiency of less than 5 percent under these conditions. Figure 4 shows a plot of the optimal drain and gate voltages as functions of output power. Two sets of data are presented, one for fixed-gate/variable-drain operation and the other for variable-gate/variable-drain operation.

The optimal drain bias for variable V_d and V_g is lower than the corresponding voltage for variable V_d only, implying a lower input DC power and higher drain efficiency. The increase in gate voltage increases g_m and thus increases gain and power-added efficiency.

Preliminary measurements were made of the transfer phase variation as a function of backoff. The results indicate a smaller phase variation, by about 30 percent, compared with fixed-voltage Class B operation. This observation is consistent with the hypothesis described earlier that the device is maintained in a state of extended saturation over a large output power range.

ANALYTIC BASIS OF THE TECHNIQUE

Under ideal fixed-voltage Class B operation, the DC input power is a function of the drain current amplitude and the drain voltage and is given by

$$P_{dc}^{B} = \frac{\Delta I}{\pi} \cdot V_d \tag{1}$$

The RF output power is given by

$$P_{out}^{B} = \frac{R_L^B \cdot \Delta I^2}{8} \tag{2}$$

where R_L^B is the Class B load resistance.

At any given drive level an optimal drain voltage exists that maximizes the output power, such that

$$V_d^{opt} = \sqrt{2 \cdot R_L^B \cdot P_{out}^B} + V_k \tag{3}$$

where V_k is the knee voltage. The knee voltage, as defined in this analysis, is not the fixed value commonly determined from a curve tracer measurement, but the drive-dependent effective value based on the onset of clipping.

From (1), (2), and (3), the drain efficiency of the ideal Class B amplifier under backoff, with fixed drain bias, becomes

$$\eta_d^{fixed} = \frac{\pi}{4} \cdot \left(\frac{1-\alpha}{1+\alpha}\right) \cdot \sqrt{\beta} \tag{4}$$

where $\alpha = \frac{V_k}{V_{bk} - V_{po}}$, and represents the FET "ideality factor," and $\beta = P_{out}/P_{out}^{max}$, the backoff ratio. Note that the drain efficiency drops, as expected for Class B, as the square root of the backoff.

For the same amplifier with optimal variable drain bias,

$$\eta_d^{var} = \frac{\pi}{4} \cdot \frac{1}{1 + \frac{2\alpha}{(1-\alpha)\cdot\sqrt{\beta}}} \tag{5}$$

The ratio of drain efficiencies of the two operating modes is now given by

$$\frac{\eta_d^{var}}{\eta_d^{fixed}} = \frac{1+\alpha}{(1-\alpha)\cdot\sqrt{\beta} + 2\alpha} \tag{6}$$

For an ideal device (α=0), the ratio is always greater than 1, indicating higher efficiency under "extended saturation" operation.

Figure 5 shows a comparison between the measured and theoretical performance of this amplifier on the basis of the

preceding analysis. In the conversion from drain efficiency to power-added efficiency for the theoretical data, the measured amplifier gains were used. The correspondence between measured and predicted performance is excellent for the first 10 dB of backoff and is still quite good up to 20 dB of backoff.

MULTISTAGE POWER AMPLIFIER PERFORMANCE

A similar experiment was conducted on a three-stage, 2-W power amplifier. The unit was first tested in a conventional fixed-bias mode and then in a mode in which the drain voltage of the two final stages was optimized for efficiency at each output level. Figure 6 shows a plot of the DC input and dissipated power versus output power for both modes. At the 2-W output level, the two modes have exactly the same characteristics, but under backoff the DC input and dissipated power for the variable V_d mode drops rapidly. In the fixed-bias case, they remain rather high and asymptotically approach the 2-W level. Figure 7 shows a plot of the efficiency of this amplifier operated in each of the two modes. The variable drain efficiency is substantially higher over the entire output power range. At 10 dB of backoff, for example, the fixed-bias efficiency is 10 percent, whereas the corresponding variable-bias efficiency is 41 percent. This represents a 4 to 1 reduction in DC power.

ACKNOWLEDGMENT

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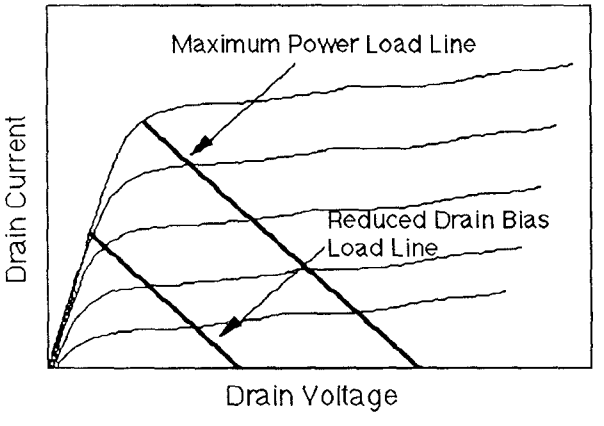

Figure 1: Maximum Power and Reduced Drain Voltage Load Lines

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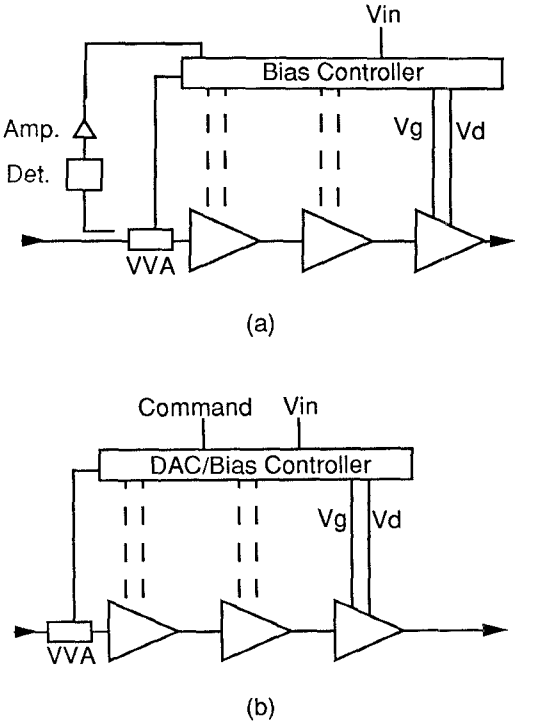

Figure 2: Drive-Controlled (a) and Externally Commanded (b) Implementations

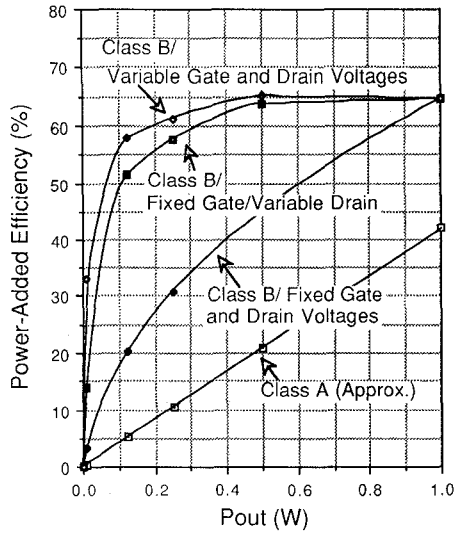

Figure 3: Measured Efficiency vs. Output Power for Several Biasing Modes

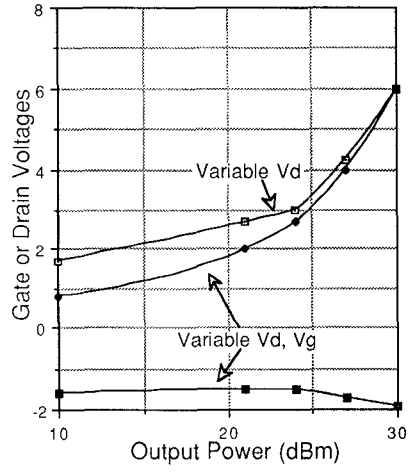

Figure 4: Optimal Drain and Gate Bias Voltages vs. Output Power

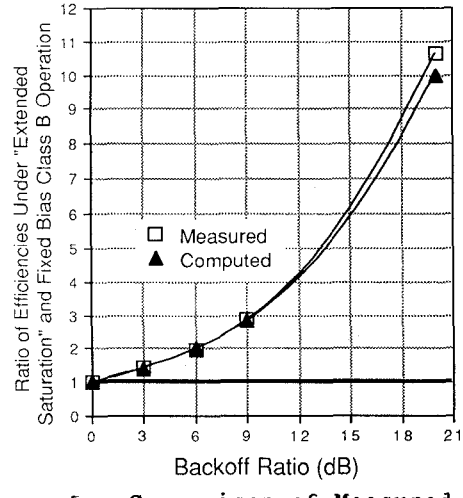

Figure 5. Comparison of Measured and Computed Efficiency Improvement

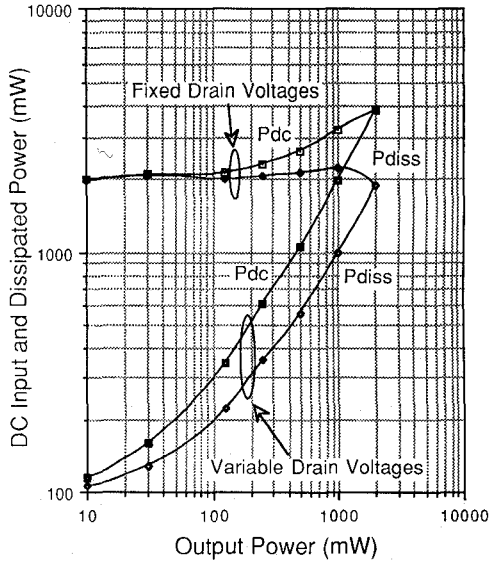

Figure 6. Measured 3-Stage Amplifier DC Input and Dissipated Powers for Two Bias Modes

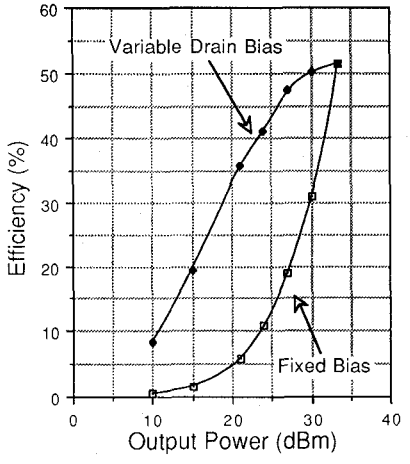

Figure 7. Measured 3-Stage Amplifier Efficiency Under Conventional and Variable Bias Modes